

## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A filter coefficient adjusting circuit comprising:
  - an FIR filter which makes an input signal subjected to a filtering process according to an equalization coefficient;
  - a PLL which extracts a clock synchronized with the input signal, using an output from the FIR filter;
  - an equalization performance detecting unit that detects an equalization performance of the FIR filter; and
  - an equalization coefficient determining unit that weights the previously-set determines the equalization coefficient of the FIR filter, for left and right taps, with respect to a center tap when the number of taps in the FIR filter is an odd number, and with respect to a central delay line when the number of taps in the FIR filter is an even number, according to an output value of the equalization performance detecting unit, and outputs the weighted value.
2. (Currently Amended) The filter coefficient adjusting circuit as defined in Claim 1 wherein

the equalization coefficient determining unit weights the equalization coefficient of the FIR filter symmetrically, with respect to a center tap when the number of taps in the FIR filter is an odd number, and with respect to a central delay line when the number of taps in the FIR filter is an even number, outputs a previously set initial value as the equalization coefficient of the FIR filter before the PLL reaches the locked state.
3. (Original) The filter coefficient adjusting circuit as defined in Claim 1 wherein

the equalization coefficient determining unit weights, while the tap coefficient of the FIR filter is an odd number, the initial value of the equalization coefficient at left with respect to a center tap of the FIR filter by a factor of n (n is a real number which is equal to 0 or larger and equal to 2 or smaller), and weights the initial value of the equalization coefficient at right by a factor of (2-n), thereby to output the weighted value.
4. (Original) The filter coefficient adjusting circuit as defined in Claim 1 wherein

the equalization coefficient determining unit weights, while the tap coefficient of the FIR filter is an even number, the initial value of the equalization coefficient at left with respect to a center of a delay line of the FIR filter by a factor of  $n$  ( $n$  is a real number which is equal to 0 or larger and equal to 2 or smaller), and weights the initial value of the equalization coefficient at right by a factor of  $(2-n)$ , thereby to output the weighted value.

5. (Original) The filter coefficient adjusting circuit as defined in Claim 3 wherein the value of weighting  $n$  is independently set for each pair consisting of two taps which are at equal distances from the center tap of the FIR filter.
6. (Original) The filter coefficient adjusting circuit as defined in Claim 4 wherein the value of weighting  $n$  is independently set for each pair consisting of two taps which are at equal distances from the center of the delay line of the FIR filter.
7. (Currently Amended) The filter coefficient adjusting circuit as defined in ~~any of Claims~~Claim 3 to 6 wherein  
the equalization coefficient determining unit determines an optimum output value of the equalization performance detecting unit, and determines the value of weighting  $n$  which provides an optimum output value of the equalization performance detecting unit.
8. (Original) The filter coefficient adjusting circuit as defined in Claim 7 wherein the equalization coefficient determining unit captures the output of the equalization performance detecting unit at variable time intervals, and determines the value of weighting  $n$  on the basis of the captured value.
9. (Original) The filter coefficient adjusting circuit as defined in Claim 7 wherein the equalization coefficient determining unit establishes an upper limit and a lower limit and an update interval thereof, independently, for the value of weighting  $n$ , and determines the value of weighting  $n$  within the established range.

10. (Original) The filter coefficient adjusting circuit as defined in Claim 7 wherein the equalization coefficient determining unit establishes an operation of detecting the value of weighting n which provides an optimum output value of the equalization performance detecting unit on the basis of the operation setting control signal in accordance with the characteristics of the input signal.
11. (New) The filter coefficient adjusting circuit as defined in Claim 4 wherein the equalization coefficient determining unit determines an optimum output value of the equalization performance detecting unit, and determines the value of weighting n which provides an optimum output value of the equalization performance detecting unit.
12. (New) The filter coefficient adjusting circuit as defined in Claim 11 wherein the equalization coefficient determining unit captures the output of the equalization performance detecting unit at variable time intervals, and determines the value of weighting n on the basis of the captured value.
13. (New) The filter coefficient adjusting circuit as defined in Claim 11 wherein the equalization coefficient determining unit establishes an upper limit and a lower limit and an update interval thereof, independently, for the value of weighting n, and determines the value of weighting n within the established range.
14. (New) The filter coefficient adjusting circuit as defined in Claim 11 wherein the equalization coefficient determining unit establishes an operation of detecting the value of weighting n which provides an optimum output value of the equalization performance detecting unit on the basis of the operation setting control signal in accordance with the characteristics of the input signal.
15. (New) The filter coefficient adjusting circuit as defined in Claim 5 wherein

the equalization coefficient determining unit determines an optimum output value of the equalization performance detecting unit, and determines the value of weighting n which provides an optimum output value of the equalization performance detecting unit.

16. (New) The filter coefficient adjusting circuit as defined in Claim 15 wherein  
the equalization coefficient determining unit captures the output of the equalization performance detecting unit at variable time intervals, and determines the value of weighting n on the basis of the captured value.
17. (New) The filter coefficient adjusting circuit as defined in Claim 15 wherein  
the equalization coefficient determining unit establishes an upper limit and a lower limit and an update interval thereof, independently, for the value of weighting n, and determines the value of weighting n within the established range.
18. (New) The filter coefficient adjusting circuit as defined in Claim 15 wherein  
the equalization coefficient determining unit establishes an operation of detecting the value of weighting n which provides an optimum output value of the equalization performance detecting unit on the basis of the operation setting control signal in accordance with the characteristics of the input signal.
19. (New) The filter coefficient adjusting circuit as defined in Claim 6 wherein  
the equalization coefficient determining unit determines an optimum output value of the equalization performance detecting unit, and determines the value of weighting n which provides an optimum output value of the equalization performance detecting unit.
20. (New) The filter coefficient adjusting circuit as defined in Claim 19 wherein  
the equalization coefficient determining unit captures the output of the equalization performance detecting unit at variable time intervals, and determines the value of weighting n on the basis of the captured value.
21. (New) The filter coefficient adjusting circuit as defined in Claim 19 wherein

the equalization coefficient determining unit establishes an upper limit and a lower limit and an update interval thereof, independently, for the value of weighting n, and determines the value of weighting n within the established range.

22. (New) The filter coefficient adjusting circuit as defined in Claim 19 wherein  
the equalization coefficient determining unit establishes an operation of detecting  
the value of weighting n which provides an optimum output value of the equalization  
performance detecting unit on the basis of the operation setting control signal in  
accordance with the characteristics of the input signal.